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INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Not for submission under 37 CFR 1.99)</i>	Application Number		10766761
	Filing Date		2004-01-28
	First Named Inventor		Craig Hampel
	Art Unit		2611
	Examiner Name		T. M. Wang
	Attorney Docket Number		RBUS 1309-1US

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
/TW/	1	5541967		1996-07-30	Gluska et al.	
/TW/	2	6691214		2004-02-10	Li et al.	
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/TW/	1	20020066001		2002-05-30	Olarig et al.	
/TW/	2	20020184461		2002-12-05	Zumkehr	
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/TW/	1	Supplementary EP Search Report for EP Patent Application 05711891.1-2415 mailed on 2007-12-18.	<input type="checkbox"/>

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<p>Substitute for form 1449B/PTO</p> <h1>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</h1> <p>(use as many sheets as necessary)</p>				Complete If Known	
Sheet	2	of	2	Application Number	10/766,761
				Filing Date	28 January 2004
				First Named Inventor	Craig E. Hampel
				Group Art Unit	2637
				Examiner Name	Jayanti K. Patel
				Attorney Docket Number	RBUS 1309-1

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Application Number	101766,761
				Filing Date	28 January 2004 (Herewith)
				First Named Inventor	Craig E. Hampel
				Group Art Unit	
				Examiner Name	
Sheet	1	of	4	Attorney Docket Number	RBUS 1309-1

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY
		Number	Kind Code ² (if known)		
/TW/	A1	4,384,354		Crawford et al.	05/17/1983
/TW/	A2	5,122,978		Merrill	06/16/1992
/TW/	A3	5,436,908		Fluker et al.	07/25/1995
/TW/	A4	5,859,881		Ferraiolo et al.	01/12/1999
/TW/	A5	6,047,346		Lau et al.	04/04/2000
/TW/	A6	6,219,384		Kliza et al.	04/17/2001
/TW/	A7	6,282,210		Rapport et al.	08/28/2001
/TW/	A8	6,359,931		Perino et al.	03/19/2002
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/TW/	A10	6,442,644		Gustavson et al.	08/27/2002
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/TW/	A17	6,556,934		Higashide	04/29/2003
/TW/	A18	6,643,787		Zerbe et al.	11/04/2003
/TW/	A19	2003/0026399		Carlson	02/06/2003

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	B3				
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(use as many sheets as necessary)				Filing Date	28 January 2004 (Herewith)
				First Named Inventor	Craig E. Hampel
				Group Art Unit	
				Examiner Name	
Sheet	2	of	4	Attorney Docket Number	RBUS 1309-1

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		Office ²	Number ⁴	Kind Code ⁵ (if known)				
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(use as many sheets as necessary)			Filing Date	28 January 2004 (Herewith)	
			First Named Inventor	Craig E. Hampel	
			Group Art Unit		
			Examiner Name		
Sheet	3	of	4	Attorney Docket Number	RBUS 1309-1

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS				
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/TW/	C1	PARIS, LLUIS ET AL, "WP 24.3 A 800MB/s 72Mb SDRAM with Digitally-Calibrated DLL," IEEE International Solid-State Circuits Conference (1999), 13 pages.		
/TW/	C2	NAKASE, YASUNOBU ET AL, "Source-Synchronization and Timing Vernier Techniques for 1.2-GB/s SDRAM Interface," IEEE Journal of Solid-State Circuits, Vol. 34, No. 4 (Apr. 1999), 494-501.		
/TW/	C3	GILLINGHAM, PETER, "SLDRAM Architectural and Functional Overview," SDRAM Consortium (29 Aug 1997), 1-14.		
/TW/	C4	"Draft Standard for a High-Speed Memory Interface (SyncLink)", Draft 0.99 IEEE P1596.7-199X (1996), 56 pages		
/TW/	C5	GILLINGHAM, PETER, "SLDRAM: High-Performance, Open-Standard Memory," IEEE (1997), 29-39		
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/TW/	C7	ZERBE, JARED ET AL, U.S. Patent Application No. 09/776,550 filed 2 February 2001, entitled "Method and Apparatus for Evaluating and Calibrating a Signaling System."		
/TW/	C8	ZERBE, JARED ET AL, U.S. Patent Application No. 09/976,170 filed 21 October 2001, entitled "Method and Apparatus for Evaluating and Optimizing a Signaling System."		
/TW/	C9	RAMBUS "Direct Rambus Short Channel Layout Guide, Version 0.95" (August 2001), 40 pages		
/TW/	C10	RAMBUS "Direct Rambus Long Channel Design Guide" (2000), 45 pages		
/TW/	C11	RAMBUS, INC. "RDRAM Direct Rambus Clock Generator" (April 2002), 22 pages		

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/TW/	C12	RDRAM® Overview, "High Performance Memory Interface Solution", Copyright 2003 Rambus, Inc., all rights reserved, 4 pages	
/TW/	C13	REDWOOD TECHNOLOGY BRIEF "High Performance Parallel Bus Interface Technology", Copyright 2003 Rambus, Inc., all rights reserved, 2 pages.	
/TW/	C14	LEWIS, DAVE, "Easy-to-Use LVDS Serdes for the Serdes Neophyte" National Semiconductor, (16 June 2003), pp. 1-5.	
/TW/	C15	INTEL "How to Measure RDRAM® System Clock Jitter" Application Note AP-667 (June 1999), pp. 1-15	

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